

## CLAIMS

We Claim

1. A data management architecture comprising:
  - a) an XOR engine;
  - b) a host network interface coupled to said XOR engine and for coupling to a host computer system;
  - c) a cache coupled to said XOR engine;
  - d) a storage device interface coupled to said cache and for coupling to a plurality of storage devices.
2. The data management architecture defined by Claim 1 wherein said XOR engine comprises:
  - a) a first transceiver coupled to said host network interface;
  - b) logic means for i) generating an XOR parity byte using said data and appending said parity byte to said data, ii) checking XOR parity, and iii) correcting detected parity errors;
  - c) a second transceiver coupled to said cache .
3. The data management architecture defined by Claim 1 wherein said host network interface comprises:
  - a) a physical interface;
  - b) a protocol engine coupled to the physical interface;
  - c) a receive buffer coupled to the protocol engine;
  - d) a transmit buffer coupled to the protocol engine;
  - e) interface buffers coupled to the transmit and receive buffers;
  - f) a bus coupled to the protocol engine;
  - g) a microcontroller coupled to the bus;
  - h) a memory coupled to the bus.

09682471.061401

4. The data management architecture defined by Claim 1 wherein said cache comprises:

a plurality of cache segments, each of said cache segments including i) a dual port memory array, ii) a bus expander coupled between said XOR engine and said dual port memory array, iii) a bus funnel coupled between said XOR engine and said dual port memory array, and iv) a buffer coupled between said storage device interface and said dual port memory.

5. The data management architecture defined by Claim 1 wherein said storage device interface comprises:

- a) a physical interface;
- b) a protocol engine coupled to the physical interface;
- c) a receive buffer coupled to the protocol engine;
- d) a transmit buffer coupled to the protocol engine;
- e) interface buffers coupled to the transmit and receive buffers;
- f) a bus coupled to the protocol engine;
- g) a microcontroller coupled to the bus;
- h) a memory coupled to the bus.

6. A data management architecture comprising:

- a) an XOR engine;
- b) a host network interface coupled to said XOR engine and for coupling to a host computer system;
- c) a cache coupled to said XOR engine;
- d) a storage device interface coupled to said cache and for coupling to a plurality of storage devices,

wherein said XOR engine includes:

a first transceiver coupled to said host network interface;

logic means for i) generating an XOR parity byte using said data and appending said parity byte to said data, ii) checking XOR parity, and iii) correcting detected parity errors;

a second transceiver coupled to said cache .

7. A data management architecture comprising:

- a) an XOR engine;
  - b) a host network interface coupled to said XOR engine and for coupling to a host computer system;
  - c) a cache coupled to said XOR engine, said cache including a plurality of cache segments, each of said cache segments including i) a dual port memory array, ii) a bus expander coupled between said XOR engine and said dual port memory array, iii) a bus funnel coupled between said XOR engine and said dual port memory array, and iv) a buffer coupled between said storage device interface and said dual port memory;
  - d) a storage device interface coupled to said cache and for coupling to a plurality of storage devices,
- wherein said XOR engine includes:
- a first transceiver coupled to said host network interface;
- logic means for i) generating an XOR parity byte using said data and appending said parity byte to said data, ii) checking XOR parity, and iii) correcting detected parity errors;
- a second transceiver coupled to said cache .

09882471.0614.01